ABSTRACT OF THE DISCLOSURE

A circuit arrangement for a power semiconductor module provides low parasitic inductances and low loss. An electrically insulating substrate supports metallic ribbon connectors which in turn power attached semiconductor components. DC port conducts are positioned in close proximity to each other and are arranged in at least one partial sector parallel and in close proximity to the surface of the substrate and/or the ribbon connectors and electrically insulated from the same, and at least one AC port conductor is similarly attached. The port conductors include surface elements enabling simplified low-inductance wire bond connection from the port conductors to either the power semiconductor components or ribbon connectors or both.